HD74LS221

Dual Monostable Multivibrators

REJ03D0458–0300
Rev.3.00
Jul.15.2005

This multivibrator features a negative-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input. Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for B input allows jitter-free triggering from inputs with transition rates as slow as 1 V/s, providing the circuit with excellent noise immunity of typically 1.2 V. A high immunity to V_{CC} noise of typically 1.5 V is also provided by internal latching circuitry. Once fired, the outputs are independent of further transitions of the A and B inputs and are a function of the timing components, or the output pulses can be terminated by the overriding clear. Input pulses may be of any duration relative to the output pulse. Output rise and fall times are TTL compatible and independent of pulse length.

Typical triggering and clearing sequence are illustrated as a part of the switching characteristics waveforms. Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature.

In most applications, pulse stability will only be limited by the accuracy of external timing components. Jitter-free operation is maintained over the full temperature and V_{CC} range for more than six decades of timing capacitance (10 pF to 10 µF) and more than one decade of timing resistance (2 kΩ to 100 kΩ).

Throughout these ranges, pulse width is defined by the relationship: $t_{w\,(out)}$ = Cext • Rext • 1n 2.

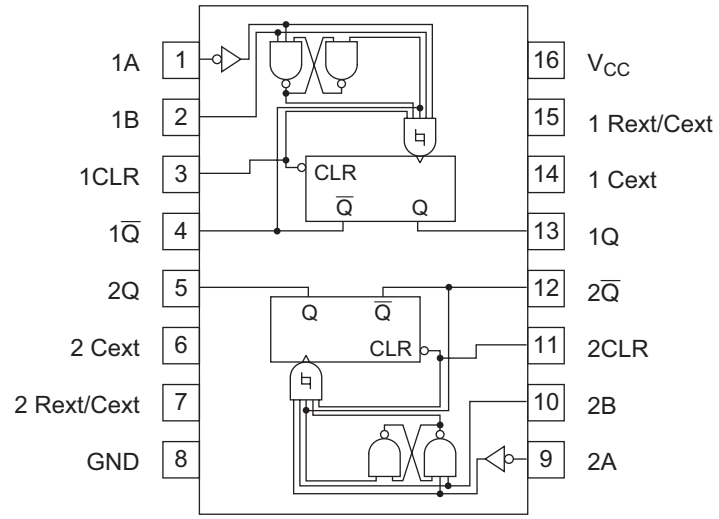
Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS221P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74LS221RPEL	SOP-16 pin (JEDEC)	PRSP0016DG-A (FP-16DNV)	RP	EL (2,500 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement



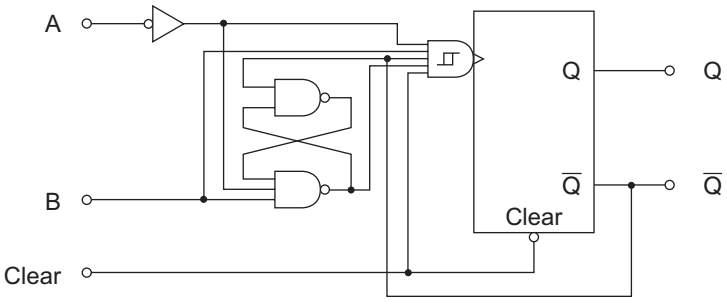
(Top view)

Function Table

Inputs			Outputs	
Clear	**A**	**B**	**Q**	**$\overline{Q}$**
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

Notes: H; high level, L; low level, X; irrelevant.
↓; Transition from high to low level.
↑; Transition from low to high level.
⎍; one high-level pulse.
⎎; one low-level pulse.

Block Diagram (1/2)



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	Tstg	–65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}	—	—	–400	µA
		I_{OL}	—	—	8	mA
Operating temperature		T_{opr}	–20	25	75	°C
Rate of rise or fall of input pulse	Schmitt input, B	dV/dt	1	—	—	V/s
	Logic Input, A		1	—	—	V/µs
Input pulse width	A or B	$t_{w\ (in)}$	40	—	—	ns
	Clear	$t_{w\ (clear)}$	40	—	—	
Setup time		t_{su}	15	—	—	ns
External timing resistance		R_{ext}	1.4	—	100	kΩ
External timing capacitance		C_{ext}	0	—	1000	µF
Duty cycle	R_T = 2 kΩ			—	50	
	R_T = 100 kΩ			—	90	

Electrical Characteristics

(Ta = –20 to +75 °C)

Item		Symbol	min.	typ.*	max.	Unit	Condition	
Threshold voltage	A	V_T^+	—	1.0	2.0	V	V_{CC} = 4.75 V	
		V_T^-	0.8	1.0	—	V	V_{CC} = 4.75 V	
	B	V_T^+	—	1.0	2.0	V	V_{CC} = 4.75 V	
		V_T^-	0.8	0.9	—	V	V_{CC} = 4.75 V	
Output voltage		V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V, I_{OH} = –400 µA	
		V_{OL}	—	—	0.4	V	I_{OL} = 4 mA	V_{CC} = 4.75 V
			—	—	0.5		I_{OL} = 8 mA	
Input current		I_{IH}	—	—	20	µA	V_{CC} = 5.25 V, V_I = 2.7 V	
	A	I_{IL}	—	—	–0.4	mA	V_{CC} = 5.25 V, V_I = 0.4 V	
	B, Clear		—	—	–0.8			
		I_I	—	—	0.1	mA	V_{CC} = 5.25 V, V_I = 7 V	
Short-circuit output current		I_{OS}	–20	—	–100	mA	V_{CC} = 5.25 V	
Supply current		I_{CC}	—	4.7	11	mA	Ouiescent	V_{CC} = 5.25 V
			—	19	27		Triggered	
Input clamp voltage		V_{IK}	—	—	–1.5	V	V_{CC} = 4.75 V, I_{IN} = –18 mA	

Note: * V_{CC} = 5 V, Ta = 25°C

Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

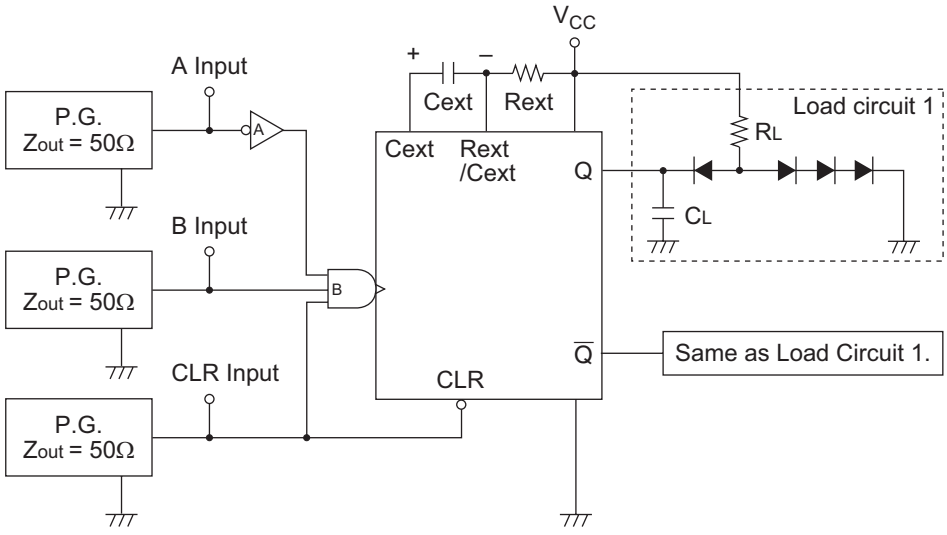
Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition	
Propagation delay time	t_{PLH}	A	Q	—	45	70	ns	C_{ext} = 80 pF, R_{ext} = 2 kΩ	C_L = 15 pF, R_L = 2 kΩ
		B	Q	—	35	55			
	t_{PHL}	A	$\overline{Q}$	—	50	80	ns		
		B	$\overline{Q}$	—	40	65			
	t_{PHL}	Clear	Q	—	35	55	ns		
	t_{PLH}	Clear	$\overline{Q}$	—	44	65	ns		
Output pulse width	$t_{w\ (out)}$	A or B	Q or $\overline{Q}$	70	120	150	ns	C_{ext} = 80 pF, R_{ext} = 2 kΩ	
				20	47	70		C_{ext} = 0 pF, R_{ext} = 2 kΩ	
				600	670	750		C_{ext} = 100 pF, R_{ext} = 10 kΩ	
				6	6.7	7.5	ms	C_{ext} = 1 μF, R_{ext} = 10 kΩ	

Caution in use

In order to prevent any malfunctions due to noise, connect a high frequency performance capacitor between Vcc and GND, and keep the wiring between the E xternal components and Cext, Rext/Cext pins as short as possible.

Testing Method

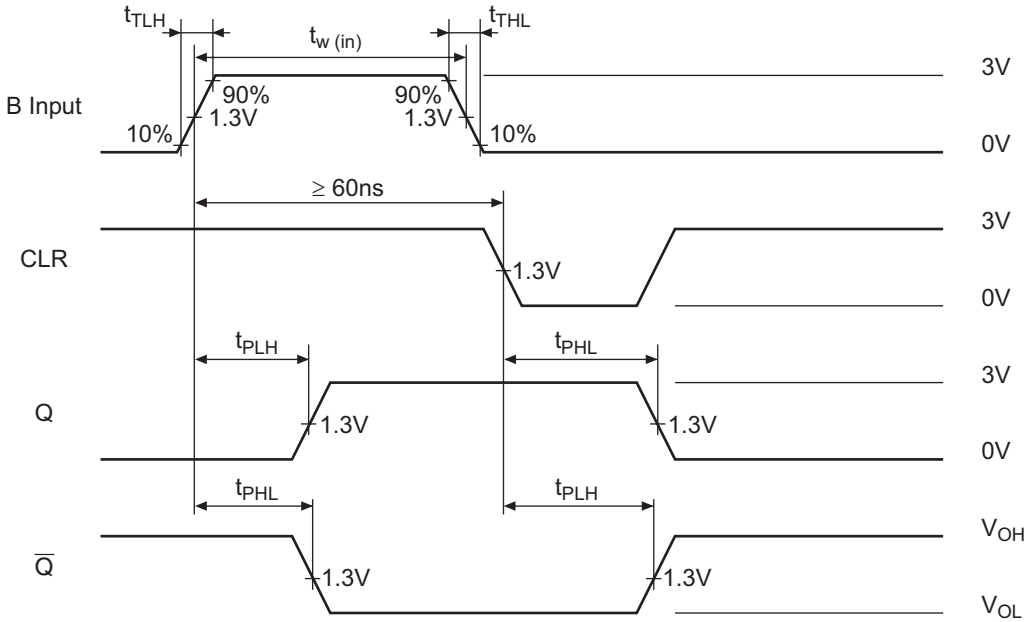
Test Circuit



Notes: 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074(H).

Waveforms 1

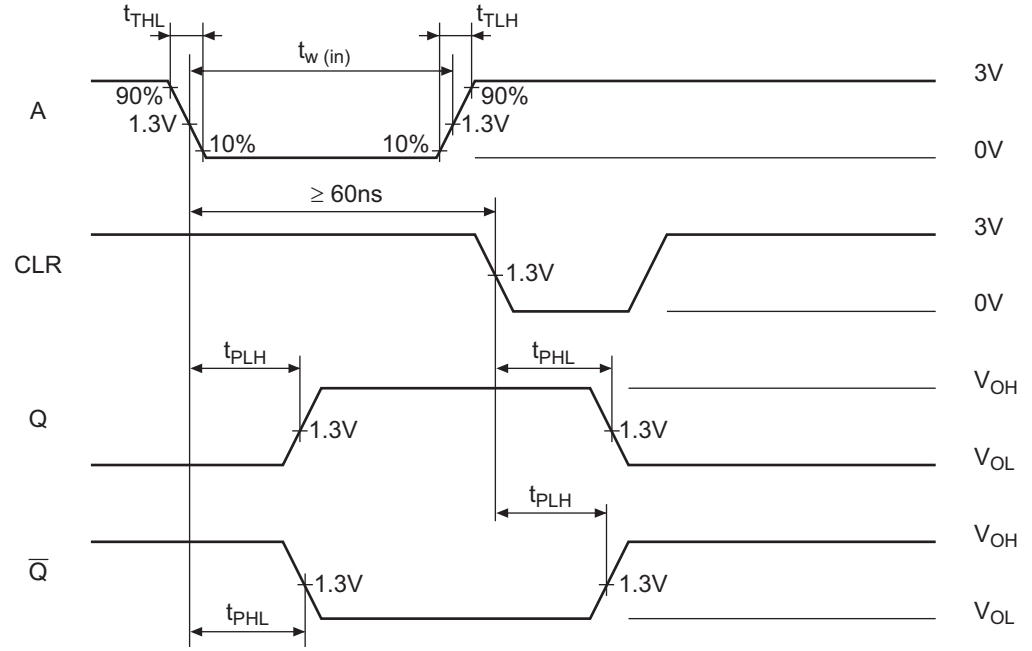
Trigger from B, then clear (A input is low).



Note: Input pulse: $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz

Waveforms 2

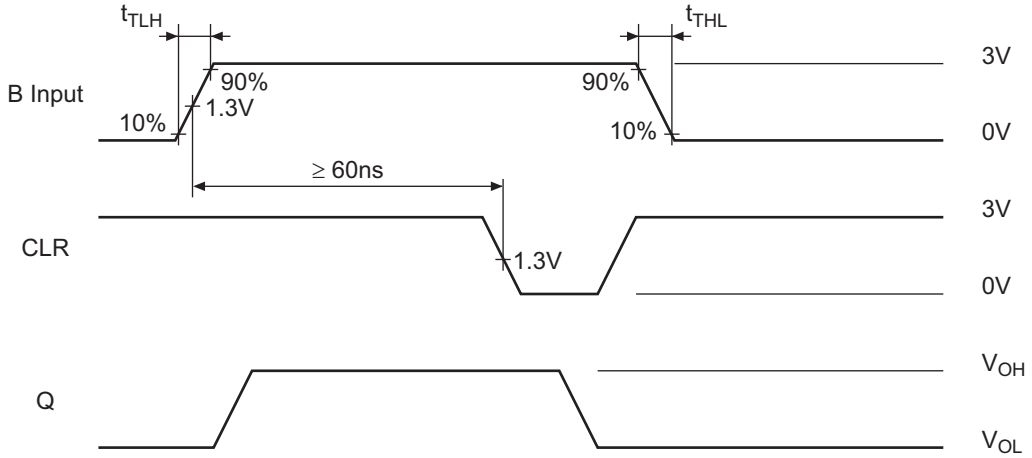
Trigger from A, then clear (B input is high).



Note: Input pulse: $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz

Waveforms 3

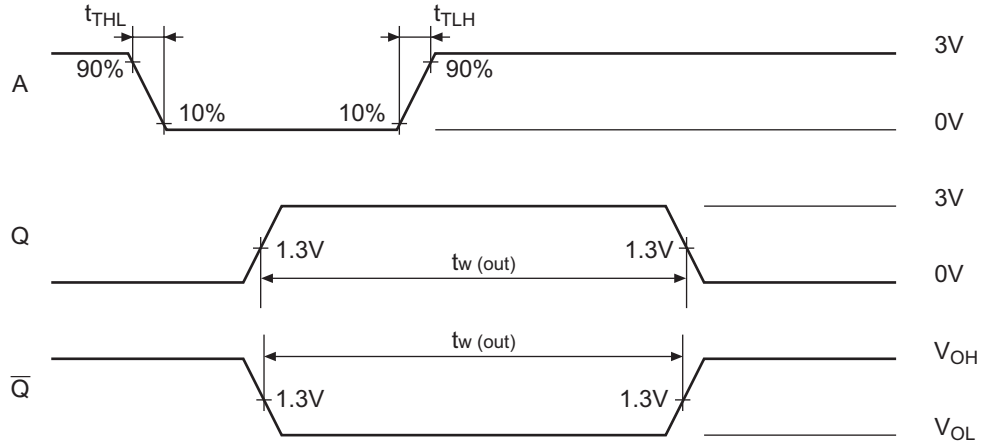
Trigger from B, then clear (A input is low).



Note: Input pulse: $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz

Waveforms 4

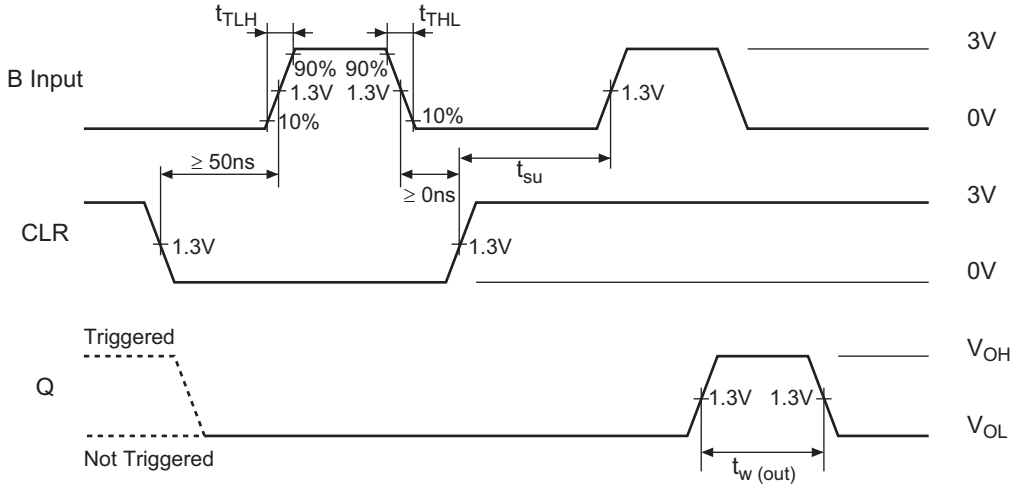
Trigger from A (B and clear input are high).



Note: Input pulse: $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz

Waveforms 5

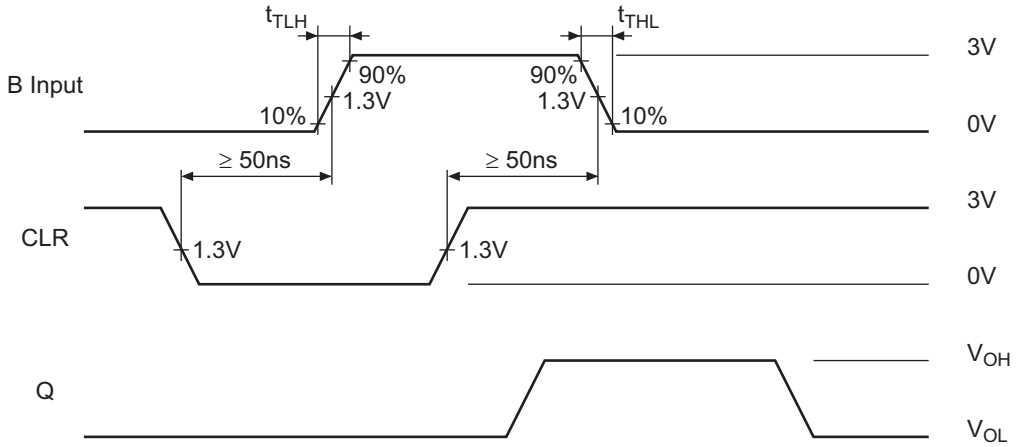
Clear overriding B, then trigger from B.



Note: Input pulse: $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz

Waveforms 6

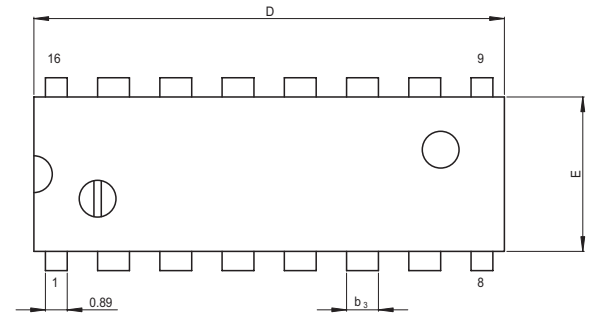
Positive transition of Clear.

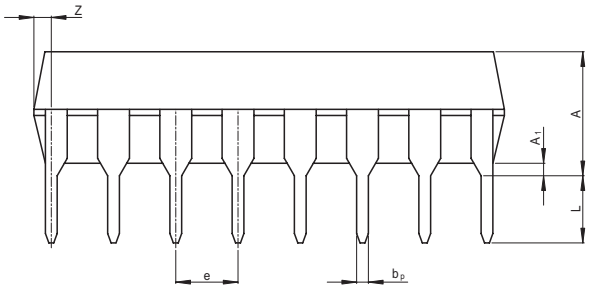


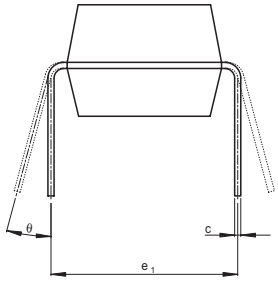
Note: Input pulse: $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP16-6.3x19.2-2.54	PRDP0016AE-B	DP-16FV	1.05g



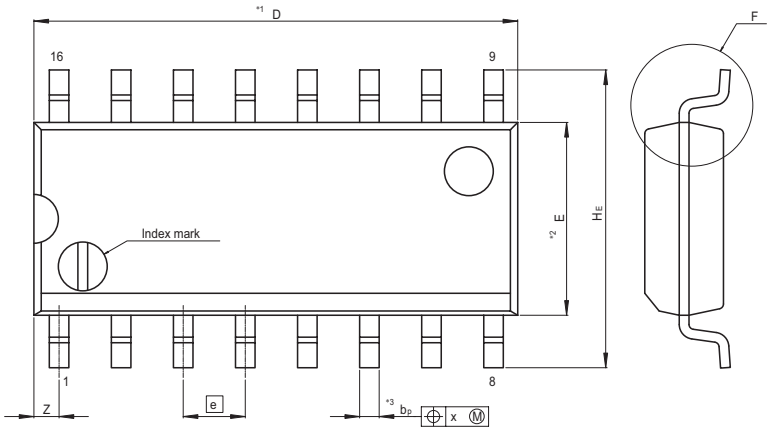


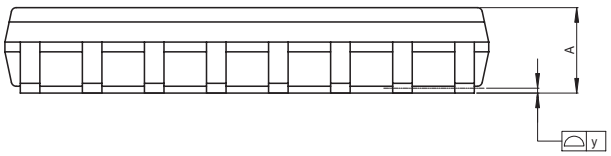


(Ni/Pd/Au plating)

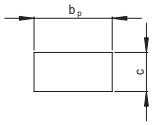
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e 1	——	7.62	——
D	——	19.2	20.32
E	——	6.3	7.4
A	——	——	5.06
A 1	0.51	——	——
b p	0.40	0.48	0.56
b 3	——	1.30	——
c	0.19	0.25	0.31
θ	0°	——	15°
e	2.29	2.54	2.79
Z	——	——	1.12
L	2.54	——	——

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-3.95x9.9-1.27	PRSP0016DG-A	FP-16DNV	0.15g

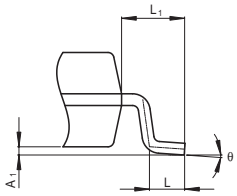




NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2"
   DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT
   INCLUDE TRIM OFFSET.



Terminal cross section
(Ni/Pd/Au plating)



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	9.90	10.30
E	——	3.95	——
A 2	——	——	——
A 1	0.10	0.14	0.25
A	——	——	1.75
b p	0.34	0.40	0.46
b 1	——	——	——
c	0.15	0.20	0.25
c 1	——	——	——
θ	0°	——	8°
H E	5.80	6.10	6.20
e	——	1.27	——
x	——	——	0.25
y	——	——	0.15
Z	——	——	0.635
L	0.40	0.60	1.27
L 1	——	1.08	——

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